**E.G.S.PILLAY ENGINEERING COLLEGE, NAGAPATTINAM.**

**DEPARTMENT OF ­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­­ ELECTICAL AND ELECTRONICS ENGINEERING**

**ACADEMIC YEAR 2014-15(ODD SEM)**



**EE6301 – DIGITAL LOGIC CIRCUITS**

**IMPORTANT 16 MARKS QUESTIONS**

**UNIT –I**

**1)Compare TTL,DTL,ECL,CMOS**

Comparison

Diagram

**2) Explain CMOS TTL in detail**

CMOS NOT explanation and diagram

TTL NAND explanation and diagram

**3) Explain in detail about error detecting and error correcting code**

Hamming code

Parity code

Even and odd parity

**UNIT-II**

**1) Simplify the boolean function using tabulation method.**

**F = \_ (0, 1, 2, 8, 10, 11, 14, 15)**

List all the min terms

Arrange them as per the number of ones based on binary equivalent

Compare one group with another for difference in one and replace the bit with dash.

Continue this until no further grouping possible.

The unchecked terms represent the prime implicants.

F = W'X'Y' + X'Z' + WY

**2) Determine the prime implicants of the function**

**F (W,X,Y,Z) = \_ (1,4,6,7,8,9,10,11,15)**

List all the min terms

Arrange them as per the number of ones based on binary equivalent

Compare one group with another for difference in one and replace the bit with dash.

Continue this until no further grouping possible.

The unchecked terms represent the prime implicants.

F = X'Y'Z + W'XZ' + W'XY + XYZ + WYZ + WX'

Minimum Set of prime implicants F = X'Y'Z + W'XZ' + XYZ + WX'

**3) Simplify the Boolean function using K-map.**

**F(A,B,C,D,E) = (0,2,4,6,9,13,21,23,25,29,31)**

Five variables hence two variable k maps one for A = 0 and the other for A = 1.

F = A'B'E' + BD'E + ACE

**4) Obtain the canonical sum of products of the function Y = AB + ACD**

Y = AB (C + C') (D + D') + ACD (B + B')

Y = ABCD + ABCD' + ABC'D + ABC'D' + AB'CD

**5) State the postulates and theorems of Boolean algebra.**

X + 0 = X X · 1 = X

X + X' = 1 X · X' = 0

X + X = X X · X = X

X + 1 = 1 X · 0 = 0

(X')' = X

X + Y = Y + X XY = YX

X + (Y + Z) = (X + Y) + Z X (YZ) = (XY) Z

X(Y + Z) = XY + XZ X + YX = (X + Y) (X + Z)

(X + Y)' = X'Y' (XY)' = X' + Y'

X + XY = X X(X + Y) = X

**6) Design a 4-bit binary adder/subtractor circuit**.

Basic equations

Comparison of equations

Design using twos complement

Circuit diagram

**7) Design a logic circuit to convert the BCD code to Excess – 3 codes.**

Truth Table for BCD to Excess – 3 conversions.

K-map simplification

Logic circuit implementing the Boolean Expression

**8) Design and explain a comparator to compare two identical words.**

Two numbers represented by A = A3A2A1A0 & B = B3B2B1B0

If two numbers equal P = Ai ⊕Bi

Obtain the logic Expression.

Obtain the logic diagram.

**9) State & prove the laws in Boolean algebra.**

**10) Simplify the three variable expression using Boolean algebra=ΠM (3, 5, 7)**

**11) Simplify the following Boolean expressions using Karnaugh map**.

(i)Y=A’C+B’C+AB’C’+A’B

(II)Y= (P’+Q+R’) (P+Q+R) (P+Q+R’)

**12) Simplify the following functions**:

(i)F(A,B,C,D)=Σ(0,1,3,8,9,13,15) (II) F(W,X,Y,Z)=Σ(0,3,4,7,9,12,14)

**13) Use a K-map technique to reduce the given expression to minimum SOP form.**

(i)Y=A’B’CD’+A’B’C’D+ABCD+ABCD’

**14) Implement the Boolean function with a mux:**

F(A,B,C,D) = Σm(0,1,3,4,8,9,15)

**15) Design a 4-bit priority encoder with input D0 having lowest priority & D3 having**

**highest priority**.

**16) Implement the Boolean function with 8:1 mux**

F (A, B, C, D) = A’BD’+ACD+B’CD+A’C’D

**17)Realize F(W’X’Y’Z) = Σ(1,4,6,7,8,9,10,11,15).**

**UNIT-III**

**1) Explain the working of BCD Ripple Counter with the help of state diagram and logic**

**Diagram.**

BCD Ripple Counter Count sequence

Truth Table

Truth Table for the J-K Flip Flop

Logic Diagram

**2)Design a sequential detector which produces an output 1 every time the input**

**sequence**

**1011 is detected.**

Construct state diagram

Obtain the flow table

Obtain the flow table & output table

Transition table

Select flip flop

Excitation table

Logic diagram

**3) Explain in detail about serial in serial out shift register**.

Block diagram

Theoretical explanation

Logic diagram

**3) Explain how one flip flop is converted to other flip flop**

Excitation table

Kmap diagram

Equation

Diagram

**UNIT-IV**

**1)What is hazards and the way to eliminate them.**

Classification of hazards

Static hazard & Dynamic hazard definitions

K map for selected functions

Method of elimination

Essential hazards

**2) State with a neat example the method for the minimization of primitive flow table.**

Consider a state diagram

Obtain the flow table

Using implication table reduce the flow table

Using merger graph obtain maximal compatibles

Verify closed & covered conditions

Plot the reduced flow table

**3) Design a asynchronous sequential circuit with 2 inputs T and C. The output attains a**

**value of 1 when T = 1 & c moves from 1 to 0. Otherwise the output is 0.**

Obtain the state diagram

Obtain the flow table

Using implication table reduce the flow table

Using merger graph obtain maximal compatibles

Verify closed & covered conditions

Plot the reduced flow table

Obtain transition table

Excitation table

Logic diagram

**4) Explain in detail about Races.**

Basics of races

Problem created due to races

Classification of races

Remedy for races

Cycles

**5) Explain the different methods of state assignment**

Three row state assignment

Shared row state assignment

Multiple row state assignment

Prevention of races.

**6)Explanation about ROM**

Classifications of ROM

Architecture of ROM

Specification of PLA

Specific Example

Related Diagram

Related Table.

**7) Implement the following using a mux. F(a,b,c,d) = \_(0,1,3,4,8,9,15)**

Obtain the truth table

From the truth table realize the expressions for the outputs and inputs

Realize the logic diagram.

**8) Explain with neat diagrams RAM architecture**.

Different Memories

Classification of memories

RAM architecture diagram

Timing waveforms

Coincident Decoding

Read write operations

**9) Explain in detail about PLA and PAL.**

Basic ROM

Classification of PROM

Logic difference between Prom & PLA

Logic diagram implementing a function

Logic difference between Prom & PAL

Logic diagram implementing a function

**10) Explain with neat diagrams a ROM architecture**.

Different Memories Classification of memories ROM architecture diagram

Timing waveforms Coincident Decoding Read write operation

**UNIT -V**

**1)** Construct a full subtractor circuit and Write a HDL program module for

the same.

(i) Compare synchronous with Asynchronous counters.

(ii) Explain the behavioral Model with suitable example.

Circuit diagram program and explanation

2) A positive edge triggered flip-flop has two inputs Dr and Dz and a control input that

chooses between the two. Write an HDL behavioral description of this flip-flop.

Circuit diagram program and explanation

3). Write an HDL behavioral description of ripple counter

Circuit diagram program and explanation

4) Write a HDL program module for full adder circuit.

Circuit diagram program and explanation

5) Write a HDL program for four bit ripple carry adder.

Circuit diagram program and explanation